## REMARKS

Claims 1-16 are presented for examination.

The Examiner has acknowledged the Information Disclosure Statement "submitted on 12/10/2003." However, the PTO-1449 form is not attached to the Office Action. It appears that the Examiner acknowledged the IDS filed on April 3, 2001 and resubmitted together with a Response filed on December 10, 2003. The Examiner is respectfully requested to provide the PTO-1449 form acknowledging consideration of the IDS filed on April 3, 2001.

Further, the Examiner is respectfully requested to provide the PTO-1449 form acknowledging consideration of the IDS filed on January 8, 2004.

*REJECTION OF CLAIMS 1-13*

Claims 1-13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Motomura.

Claims 11-13 have been cancelled without prejudice or disclaimer.

Claim 1 has been amended to more clearly define the invention over the reference. Claim 1, as amended, recites a semiconductor memory device, comprising:

- a terminal group receiving an externally applied control signal, address, and data;

- a memory cell array including a plurality of memory cells arranged in rows and columns;

- a logic circuit processing data in accordance with at least one of said control signal, said address, and said data when said address applied to said terminal group designates a prescribed first region of said memory cell array; and

- a memory circuit transmitting/receiving said data to/from a memory cell corresponding to said address in said memory cells array in accordance with said control signal and said address



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when said address applied to said terminal group designates a region except said prescribed first region.

Motomura does not teach or suggest the logic circuit and the memory circuit arranged and operating in the manner required by claim 1. In particular, Motomura does not disclose a memory circuit transmitting/receiving data to/from a memory cell corresponding to an address in a memory cells array in accordance with a control signal and the address when the address applied to the terminal group designates a region except the prescribed first region.

Further, the Examiner considers the control section 12 of Motomura to correspond to the claimed logic circuit. The Examiner relies upon col. 31, lines 17-20, col. 7, lines 57-59 and col. 8, lines 14-16 for disclosing that the memory sections 11 are designated by the parameter field which designates the address of data in the DRAM core section 15.

Considering the reference, Motomura discloses that the parameter field in the request packet designates a memory control register 29 to which access is performed (col. 31, lines 17-20). Further, the reference discloses that the parameter field may be used for designation of address of data in the DRAM core section 15 (col. 7, lines 57-59, col. 8, lines 14-16).

Hence, Motomura does not disclose that the control section 12 processes data when address applied to the terminal group designates a prescribed first region of the memory cell array, as claim 1 requires.

Accordingly, as demonstrated above, Motomura does not teach or suggest a logic circuit processing data in accordance with at least one of the control signal, the address, and the data when the address applied to the terminal group designates a prescribed first region of the memory cell array; and a memory circuit transmitting/receiving the data to/from a memory cell corresponding to the address in the memory cells array in accordance with the control signal and



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the address when the address applied to the terminal group designates a region except the prescribed first region, as claim 1 recites.

Claims 2-10 are defined over the reference at least for the reasons presented above in connection with claim 1. Therefore, the amendment to claim 1 overcomes the rejection of claims 1-10 under 35 U.S.C. § 102.

*REJECTION OF CLAIMS 14-16*

Claims 14-16 have been rejected under 35 U.S.C. § 103 as being unpatentable over Motomura in view of Mori et al. This rejection is respectfully traversed for the following reasons.

It is noted that claim 14 has been amended to rephrase the claimed language. It is submitted that the claim amendment does not narrow the scope of the claim for reasons related to the outstanding rejection or the statutory requirements for a patent.

Independent claim 14 recites a semiconductor memory device, comprising:

- a first terminal group receiving an externally applied control signal, address, and data;

- a memory including a plurality of memory cells arranged in rows and columns and activated in accordance with an externally applied select signal for transmitting/receiving said data in accordance with said control signal with respect to a memory cell in a region designated by said address;

- a logic circuit activated in accordance with said select signal in a complementary manner with respect to said memory for processing data in accordance with at least one of said address and said data; and

- a second terminal receiving said select signal.

The Examiner holds Motomura to differ from the claimed invention in that the reference does not disclose the logic circuit activated in accordance with said select signal in a complementary manner with respect to said memory for processing data in accordance with at least one of said address and data. Mori is relied upon for disclosing these features.

First, as discussed above, it appears that Motomura does not disclose a memory array activated in accordance with the select signal for transmitting/receiving the data in accordance with the control signal with respect to a memory cell in a region designated by the address.

Further, Mori does not disclose a select signal for transmitting/receiving data in accordance with the control signal with respect to a memory cell in a region designated by the address. Therefore, this reference cannot disclose a logic circuit activated in accordance with such a select signal in a complementary manner.

It is well settled that the test for obviousness is what the combined teachings of the references would have suggested to those having ordinary skill in the art. ***Cable Electric Products, Inc. v. Genmark, Inc.***, 770 F.2d 1015, 226 USPQ 881 (Fed. Cir. 1985). In determining whether a case of prima facie obviousness exists, it is necessary to ascertain whether the prior art teachings appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification. ***In re Lalu***, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984).

As discussed above, the combined teachings of the references are not sufficient to arrive at the logic circuit activated in accordance with an externally applied select signal for transmitting/receiving data in accordance with the control signal with respect to a memory cell in a region designated by the address, in a complementary manner with respect to the memory for processing data in accordance with at least one of the address and the data. Therefore, the Examiner's conclusion of obviousness is not warranted.



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Moreover, it is incumbent upon the Examiner to provide a basis in fact and/or cogent technical reasoning to support the conclusion that one having ordinary skill in the art would have been motivated to combine references to arrive at a claimed invention. ***Uniroyal, Inc. v. Rudkin-Wiley Corp.***, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

However, the Examiner offered no logical reason, and no such reason is apparent, to support the conclusion that one having ordinary skill in the art would have been impelled to modify Motomura by utilizing a teaching of Mori.

The Examiner takes the position that such a modification would reduce "a wasteful output current of the power supply circuit since the unnecessary applying period of an overdriving voltage to transistors is reduced." However, Motomura does not appear to suffer from wasting output current of the power supply circuit. Moreover, Motomura does not even recognize an existence of "the unnecessary applying period of an overdriving voltage to transistors."

Therefore, it is not apparent why one skilled in the art would have recognized any advantage to be gained by the proposed combination of references. Hence, there is no motivation for modifying Motomura in accordance with the Examiner's suggestion.

Accordingly, the Examiner has failed to provide the requisite reasons for modifying the reference and thus to establish a *prima facie* case of obviousness.

Accordingly, Applicants submit that the lack of any motivation for the proposed combination of references to arrive at the claimed invention, coupled with the absence of teachings or suggestions in the references of the claimed invention, undermine the basis for the Examiner's rejection under 35 U.S.C. § 103. Applicants, therefore, respectfully request that the rejection of claims 14-16 under 35 U.S.C. § 103 is improper and should be withdrawn.



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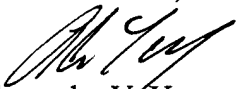
In view of the foregoing, and in summary, claims 1-10 and 14-16 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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